Complete Listing of the Claims

Upon entry of the present amendment, the claims will stand as follows. The following listing of claims will replace all prior versions and listings of the claims in the present application:

Please amend the claims of the above-identified patent application as follows:

1. (Currently amended) A semiconductor substrate comprising:

a monocrystalline silicon-containing material having a surface substantially free of oxidation; and

an organic layer having more than half of its atoms being carbon and hydrogen, wherein the organic layer is chemically bonded to the surface of the silicon-containing material, wherein an electrical property selected from surface recombination velocity, carrier lifetime, electronic efficiency, voltage, device capacitance, contact resistance and resistance of a doped region of the semiconductor substrate is improved as compared to the electrical property of the substrate in the absence of the organic layer, and

wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises a measurable carrier lifetime for low-level injection of more than approximately 7.8 μs or for high-level injection of more than approximately 12 μs, or a measurable surface recombination velocity of less than approximately 1300 cm/s for low-level injection or less than approximately 810 cm/s for high-level injection.

2. (Canceled) The electrical structure of claim 1, wherein the organic layer affects the electrical property within the silicon-containing material.

3. (Canceled) The electrical structure of claim 2, wherein the electrical property is selected from a group consisting of a surface recombination velocity, carrier lifetime, electronic efficiency, voltage, device capacitance, contact resistance, and resistance of a doped region.

4. (Previously amended) The semiconductor substrate of claim 1, wherein the organic layer comprises a hydrocarbon.

5. (Previously amended) The semiconductor substrate of claim 1, wherein the organic layer comprises a polymer.

6. (Withdrawn) The electrical structure of claim 1, wherein:

the silicon-containing material is at least part of a photovoltaic cell; and

the silicon-containing material comprises a region at the surface, wherein the region has a dopant concentration of at least approximately 1E19 atoms per cubic centimeter.

7. (Withdrawn) The electrical structure of claim 1, wherein:

the silicon-containing material is at least part of a channel region of a field-effect transistor; and

the organic layer is at least part of a gate dielectric for the field-effect transistor.

8. (Withdrawn) The electrical structure of claim 1, further comprising a high-k material wherein:

the silicon-containing material is at least part of a channel region of a field-effect transistor;

the organic layer lies between the silicon-containing material and the high-k material; and

the high-k material is at least part of a gate dielectric for the field-effect transistor.

9. (Canceled) The electrical structure of claim 1, wherein the silicon-containing material is substantially monocrystalline.

10. (Canceled) The electrical structure of claim 1, wherein the silicon-containing material is polycrystalline.

11. (Currently amended) The semiconductor substrate of claim 1, ~~wherein the silicon-containing material is~~ further comprising a substantially amorphous silicon containing-material.

12. (Currently amended) The semiconductor substrate of claim 1, ~~wherein~~ further comprising a ~~portion of the~~ porous silicon-containing material immediately adjacent to the organic layer that has a porosity no greater than approximately 30 percent.

13. (Currently amended) A process for forming a semiconductor substrate, comprising:

providing a monocrystalline silicon-containing material having a surface substantially free of oxidation; and

forming an organic layer having more than half of its atoms being carbon and hydrogen, wherein the organic layer is chemically bonded to the surface of the silicon-containing material, wherein an electrical property selected from surface recombination velocity, carrier lifetime, electronic efficiency, voltage, device capacitance, contact resistance, and resistance of a doped region of the semiconductor substrate is changed as compared to the electrical property of the substrate in the absence of the organic layer, thereby forming a semiconductor substrate, and

wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises a measurable carrier lifetime for low-level injection of more than approximately 7.8 μs or for high-level injection of more than approximately 12 μs, or a measurable surface recombination velocity of less than approximately 1300 cm/s for low-level injection or 810 cm/s for high-level injection.

14. (Canceled) The process of claim 13, wherein the organic layer affects the electrical property within the silicon-containing material.

15. (Canceled) The process of claim 14, wherein the electrical property is selected from a group consisting of ~~an~~ surface recombination velocity, carrier lifetime, electronic efficiency, voltage, contact resistance, and resistance of a doped region.

16. (Original) The process of claim 13, wherein the organic layer comprises a monolayer.

17. (Original) The process of claim 13, wherein the organic layer comprises a polymer.

18. (Withdrawn) The process of claim 13, further comprising doping a portion of the silicon-containing material at the surface, wherein:

the portion has a dopant concentration of at least approximately $1x10^{19}$ atoms per cubic centimeter immediately adjacent to the surface;

the silicon-containing material is at least part of a photovoltaic cell; and

doping is performed before forming the organic layer.

19. (Withdrawn) The process of claim 13, further comprising forming a gate electrode over the organic layer, wherein:

the silicon-containing material is at least part of a channel region of a field-effect transistor;

the organic layer is at least part of a gate dielectric for the field-effect transistor; and

the gate electrode is a control electrode for the field-effect transistor.

20. (Withdrawn) The process of claim 13, further comprising:

forming a high-k material; and

forming a gate electrode, wherein:

the silicon-containing material is at least part of a channel region of a field-effect transistor;

the organic layer lies between the silicon-containing material and the high-k material; and

the high-k material is at least part of a gate dielectric for the field-effect transistor and lies between the silicon-containing material and the gate electrode.

21. (Original) The process of claim 13, wherein forming the organic layer comprises:

activating the surface of the silicon-containing material to form an activated surface;

reacting the activated surface with a chemical, wherein during the reaction, a hydrocarbon group becomes chemically bonded to the silicon-containing material.

22. (Original) The process of claim 21, wherein activating comprises halogenating the surface of the silicon-containing material to form the activated surface.

23. (Original) The process of claim 22, wherein the hydrocarbon group has no more than nine carbon atoms.

24. (Original) The process of claim 23, wherein the hydrocarbon group is an alkyl group.

25. (Original) The process of claim 21, wherein the hydrocarbon group is an allyl group.

26. (Original) The process of claim 21, further comprising forming a polymer layer from the allyl group.

27. (Original) The process of claim 21, wherein the hydrocarbon group is an alkoxide group.

28. (Canceled) The process of claim 13, wherein the silicon-containing material is substantially monocrystalline.

29. (Canceled) The process of claim 13, wherein the silicon-containing material is polycrystalline.

30. (Currently amended) The process of claim 13, ~~wherein~~ further comprising providing ~~the silicon-containing material is~~ a substantially amorphous silicon-containing material.

31. (Withdrawn) A process for forming an electrical device comprising:

forming a patterned insulating layer over at least of the electrical device, wherein:

the patterned insulating layer defines an opening;

a silicon-containing region has an exposed portion at the opening; and

the silicon-containing region is at least part of an electrical component within the electrical device;

forming an organic layer chemically bonded to the surface of the silicon-containing region;

removing the organic layer; and

forming a metal-containing layer after removing the organic layer, wherein at least a portion of the metal-containing layer contacts the exposed portion of the silicon-containing region, and wherein the metal-containing layer is part of an electrical connection to the silicon-containing region.

32. (Withdrawn) The process of claim 31, further comprising allowing at least approximately four hours to elapse between forming the organic layer and removing the organic layer.

33. (Withdrawn) The process of claim 31, further comprising annealing the non-insulating layer to form a metal silicide from the metal-containing layer and the silicon-containing region.

34. (Withdrawn) The process of claim 31, wherein no etching act is performed between forming and removing the organic layer.

35. (Withdrawn) A process for forming an electrical device comprising:

forming a patterned insulating layer over at least of the electrical device, wherein:

the patterned insulating layer defines an opening;

a silicon-containing region has an exposed portion at the opening; and

the silicon-containing region is at least part of an electrical component within the electrical device;

forming an organic layer chemically bonded to the surface of the crystalline material;

removing the organic layer; and

forming a dopant-source layer that contacts the exposed portion of the silicon-containing region.

36. (Withdrawn) The process of claim 35, further comprising allowing at least approximately four hours to elapse between forming the organic layer and removing the organic layer.

37. (Withdrawn) The process of claim 35, wherein the dopant-source layer comprises at least approximately 90 percent of at least one Group IVA element.

38. (Withdrawn) The process of claim 35, further comprising annealing the dopant-source layer to diffuse at least a portion of the dopant atoms into the silicon-containing region.

39. (Withdrawn) The process of claim 35, wherein no etching act is performed between forming and removing the organic layer.

40. (Withdrawn) An electrical structure comprising:

a silicon-containing material having a surface and at least one electrode, wherein the silicon-containing material is capable of conducting electric current, and

an organic layer chemically bonded to the surface of the silicon-containing material, wherein an electrical property of the electrical structure is significantly improved compared to a same structure without the organic layer.

41. (Previously amended) The semiconductor substrate of claim 1, wherein the structure without the organic layer comprises a silicon-containing material having a surface, wherein the surface is a hydrogen terminated surface.

42. (Canceled) The electrical structure of claim 1, wherein the structure without the organic layer comprises a silicon-containing material having a surface, wherein the surface is an oxidized surface.

43. (New) The process of claim 13, further comprising providing a porous silicon-containing material immediately adjacent to the organic layer that has a porosity no greater than approximately 30 percent.

44. (New) The silicon substrate of claim 1, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises a methylated surface with measurable carrier lifetimes for low-level injection of at least approximately 260 μs or for high-level injection of at least approximately 290 μs, or with measurable surface recombination velocities of not more than approximately 17 cm/s for low-level injection or 21 cm/s for high-level injection, or combinations thereof.

45. (New) The silicon substrate of claim 1, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises an ethylated surface with measurable carrier lifetimes of more than approximately 40 μs, or with measurable surface recombination velocities of less than approximately 350 cm/s, or both.

46. (New) The silicon substrate of claim 1, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises an ethylated surface with measurable carrier lifetimes of more than approximately 30 μs, or with measurable surface recombination velocities of less than approximately 470 cm/s, or both.

47. (New) The silicon substrate of claim 1, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises a hexylated, octylated or dodecylated surface with measurable carrier lifetimes of at least approximately 20 μs, or with measurable surface recombination velocities of not more than approximately 200 cm/s, or both.

48. (New) The silicon substrate of claim 1, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises an

alkoxylated surface with measurable carrier lifetimes of more than approximately 150 μs for low-level injection or more than approximately 140 μs for high-level injection, or with measurable surface recombination velocities of not more than approximately 70 cm/s, or combinations thereof.

49. (New) The process of claim 13, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises a methylated surface with measurable carrier lifetimes for low-level injection of at least approximately 260 μs or for high-level injection of at least approximately 290 μs, or with measurable surface recombination velocities of not more than approximately 17 cm/s for low-level injection or 21 cm/s for high-level injection, or combinations thereof.

50. (New) The process of claim 13, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises an ethylated surface with measurable carrier lifetimes of more than approximately 40 μs, or with measurable surface recombination velocities of less than approximately 350 cm/s, or both.

51. (New) The process of claim 13, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises an ethylated surface with measurable carrier lifetimes of more than approximately 30 μs, or with measurable surface recombination velocities of less than approximately 470 cm/s, or both.

52. (New) The process of claim 13, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises a hexylated, octylated or dodecylated surface with measurable carrier lifetimes of at least approximately 20 μs, or with measurable surface recombination velocities of not more than approximately 200 cm/s, or both.

53. (New) The process of claim 13, wherein as a result of said organic layer being chemically bonded to the surface of the silicon-containing material, said surface comprises an alkoxylated surface with measurable carrier lifetimes of more than approximately 150 μs for low-level injection or more than approximately 140 μs for high-level injection, or with measurable surface recombination velocities of not more than approximately 70 cm/s, or combinations thereof.